No. 1719 P. 7

Appl. No. 09/841,582 Amdt. Dated April 17, 2006

Reply to Office Action of October 17, 2005

## **AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-5. (Cancelled)

6. (Currently Amended) A pseudo wafer comprising a plurality of

semiconductor chips each having at least their electrodes formed solely on one surface

thereof, wherein interspaces between each individual one of said chips and bottom surfaces

thereof are continuously covered with said protective material, and the chips are bonded with

each other via the protective material and further wherein the protective material adjacent the

side surfaces of each semiconductor chip is cut to provide substantially vertical side walls of

protective material formed adjacent the sides of the semiconductor chips, there being

substantially none of the protective material formed on the one surface at which the

electrodes are formed, the electrodes being covered with a solder material for forming a

solder ball.

7. (Original) The pseudo wafer according to claim 6 wherein said protective

material comprises either one of an organic insulating resin and an inorganic insulating

material.

8. (Previously Presented) The pseudo wafer according to claim 6 wherein said

plurality of semiconductor chips arrayed thereon are diced at a position of said protective

Apr. 17. 2006 10:03PM Trexler Bushnell et al No. 1719 P. 8

Appl. No. 09/841,582 Amdt. Dated April 17, 2006 Reply to Office Action of October 17, 2005

material between said plurality of semiconductor chips and thereafter mounted on a packaging substrate such that the protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip.

9. (Original) The pseudo wafer according to claim 8 wherein a solder bump is formed on said electrode.